

CLAIMS:

1. Digital signal processing apparatus comprising a plurality of available hardware resource means and a first instruction set means having access to said available hardware resource means, so that at least a part of said hardware resource means execute operations under control of said first instruction set means;

5 characterized by a second instruction set means having access to only a predetermined limited subset of said plurality of available hardware resource means, so that at least a part of said predetermined limited subset of said hardware resource means execute operations under control of said second instruction set means.

10 2. Apparatus according to claim 1, wherein said available hardware resource means are processor resource means.

3. Apparatus according to claim 1 or 2, comprising first state buffer means for storing the current state of hardware resource means in case of an interrupt,
15 characterized in that in case of an interrupt said first state buffer means stores the current state of at least a part of such hardware resource means which are not included in said predetermined limited subset of said hardware resource means.

4. Apparatus according to claim 3,
20 characterized by second state buffer means for storing in case of an interrupt the current state of at least a part of said predetermined limited subset of said hardware resource means, said second state buffer means having a smaller size than that of said first state buffer means.

25 5. Apparatus according to claim 4, comprising means for supplying power to said second state buffer means, characterized in that said power supply means essentially supplies power to said second state buffer means only during interrupt handling.

6. Apparatus according to claim 4 or 5, characterized in that at least a part of such hardware resource means which are not directly accessible and not included in said predetermined limited subset of said hardware resource means are chained together in a first scan chain means and at least a part of such hardware resources which are not directly
5 accessible and included in said predetermined limited subset of said hardware resource means are chained together in a second scan chain means.

7. Apparatus according to at least any one of the preceding claims, characterized in that said second instruction set means does not allow operations in parallel.
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8. Method for processing digital signals in a digital signal processing apparatus comprising a plurality of available hardware resource means wherein at least a part of said hardware resource means execute operations under control of a first instruction set; characterized in that at least a part of a predetermined limited subset of said plurality of
15 available hardware resource means execute operations under control of a second instruction set having access to only said predetermined limited subset of said hardware resource means.

9. Method according to claim 8, wherein in case of an interrupt the current state of hardware resource means are stored in first state buffer means; characterized in that in case of an interrupt the current state of at least a part of such hardware
20 resource means which are not included in said predetermined limited subset of said hardware resource means are stored in said first state buffer means.

10. Method according to claim 9, characterized in that in case of an interrupt the current state of at least a part of said
25 predetermined limited subset of said hardware resource means are stored in a second state buffer means having a smaller size than that of said first state buffer means.

11. Method according to claim 10, characterized is that power is essentially supplied to said second state buffer means only
30 during interrupt handling.

12. Method according to at least any one of claims 8 to 11, characterized in that said second instruction set does not allow operations in parallel.